

Equalized block

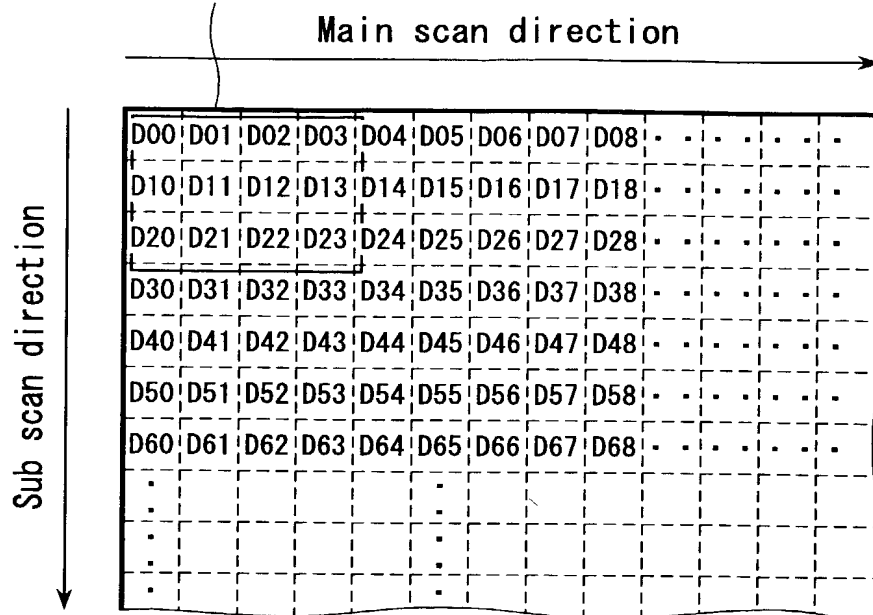


FIG. 1A

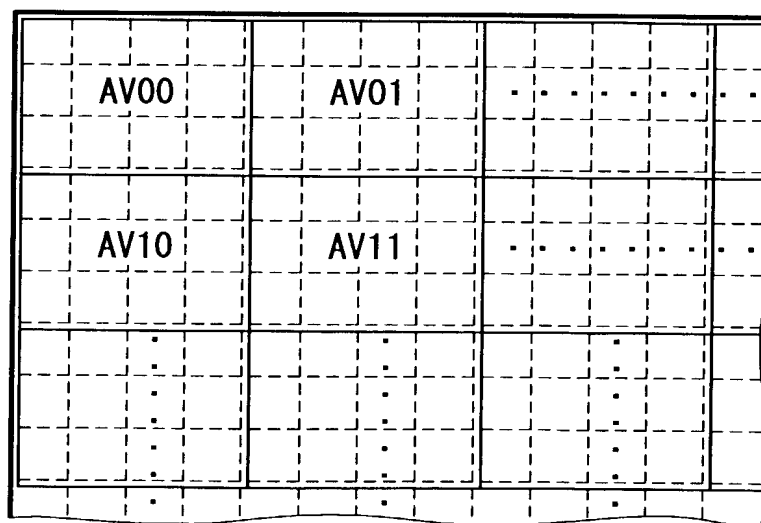


FIG. 1B

Title: Equalizing Circuit And Method, And
Image Processing Circuit And Method
Inventor: Hiroki SATOH
Appl. No.: 10/055,402

Equalizing start position

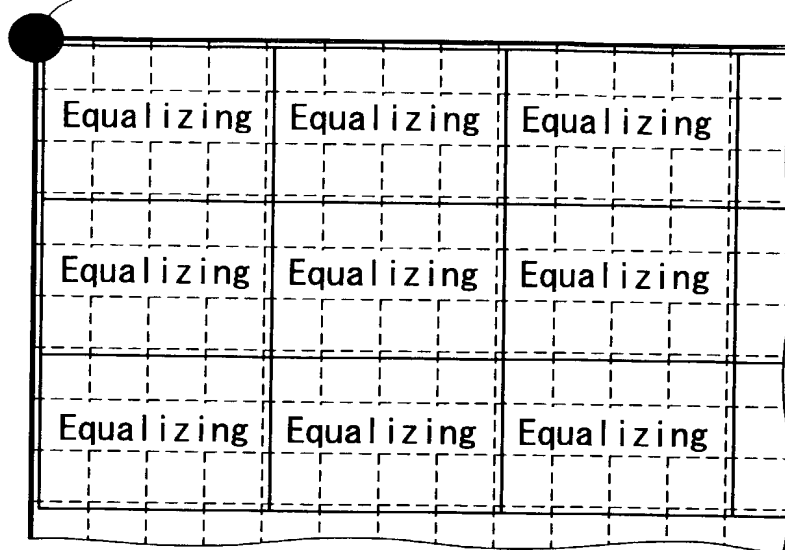


FIG. 2A

Equalizing start position

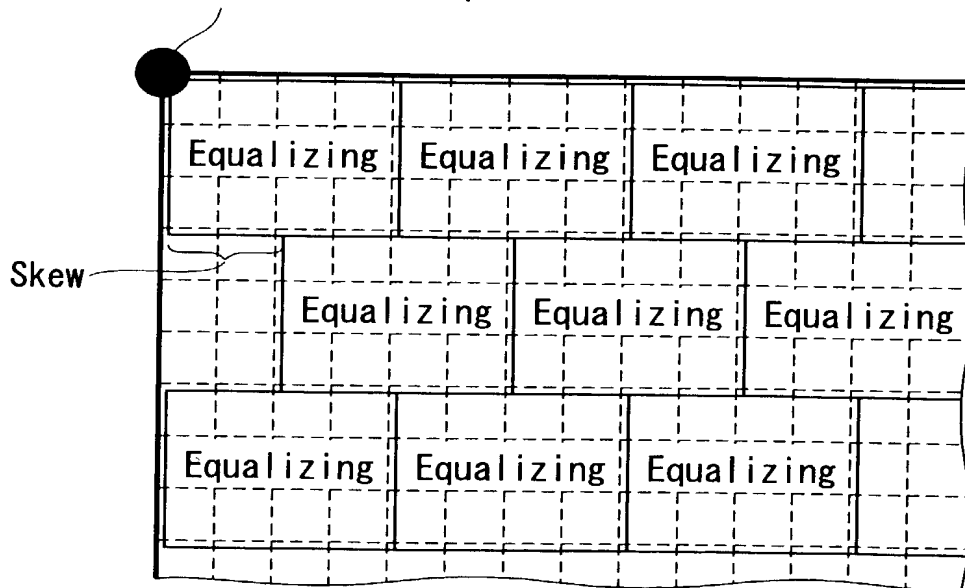


FIG. 2B

Equalizing start position

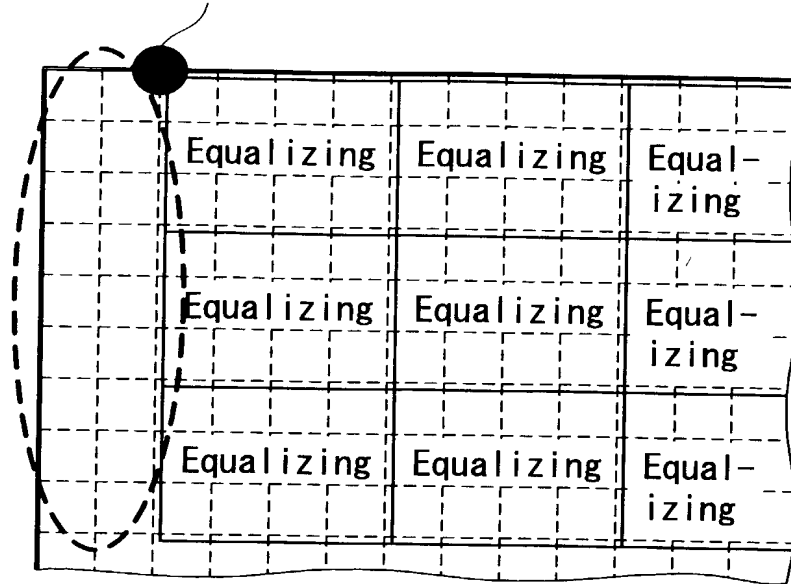


FIG. 3A

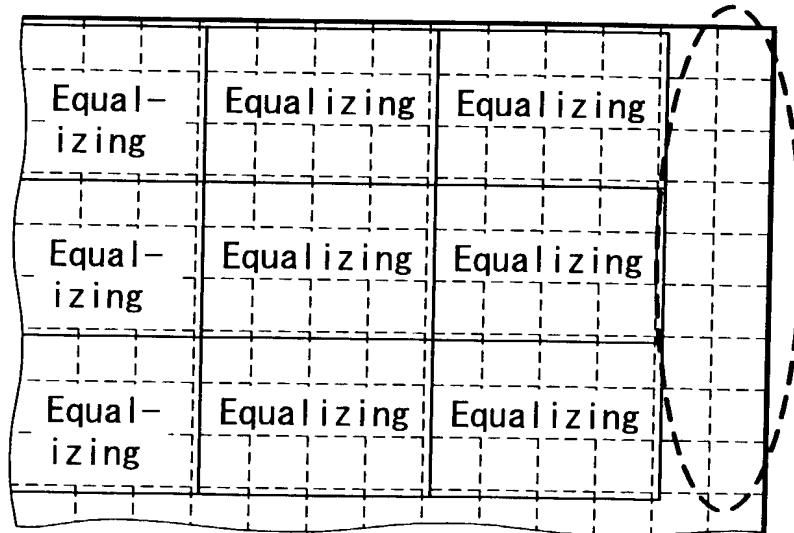


FIG. 3B

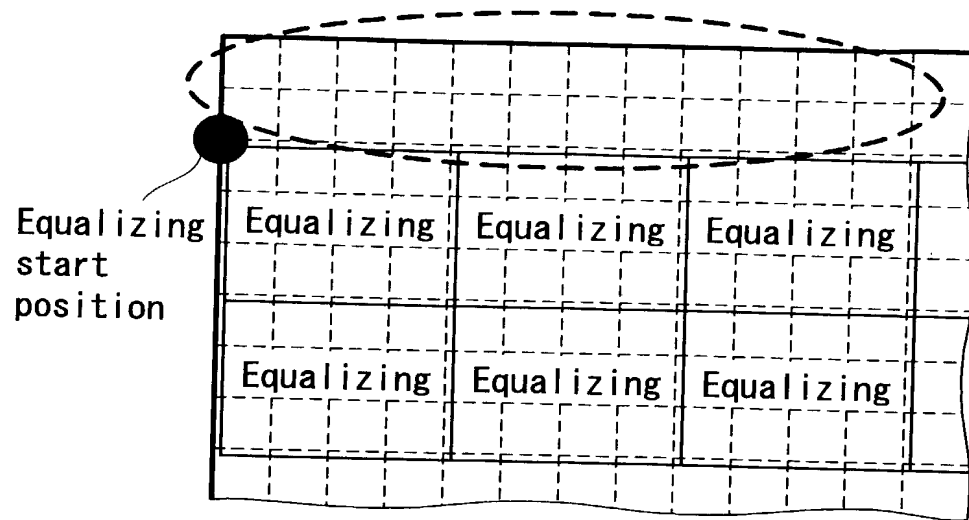


FIG. 3C

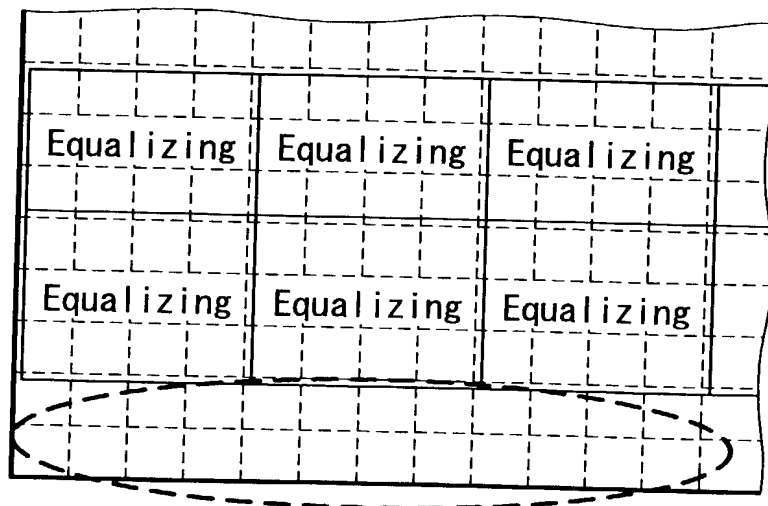


FIG. 3D



Main scan direction

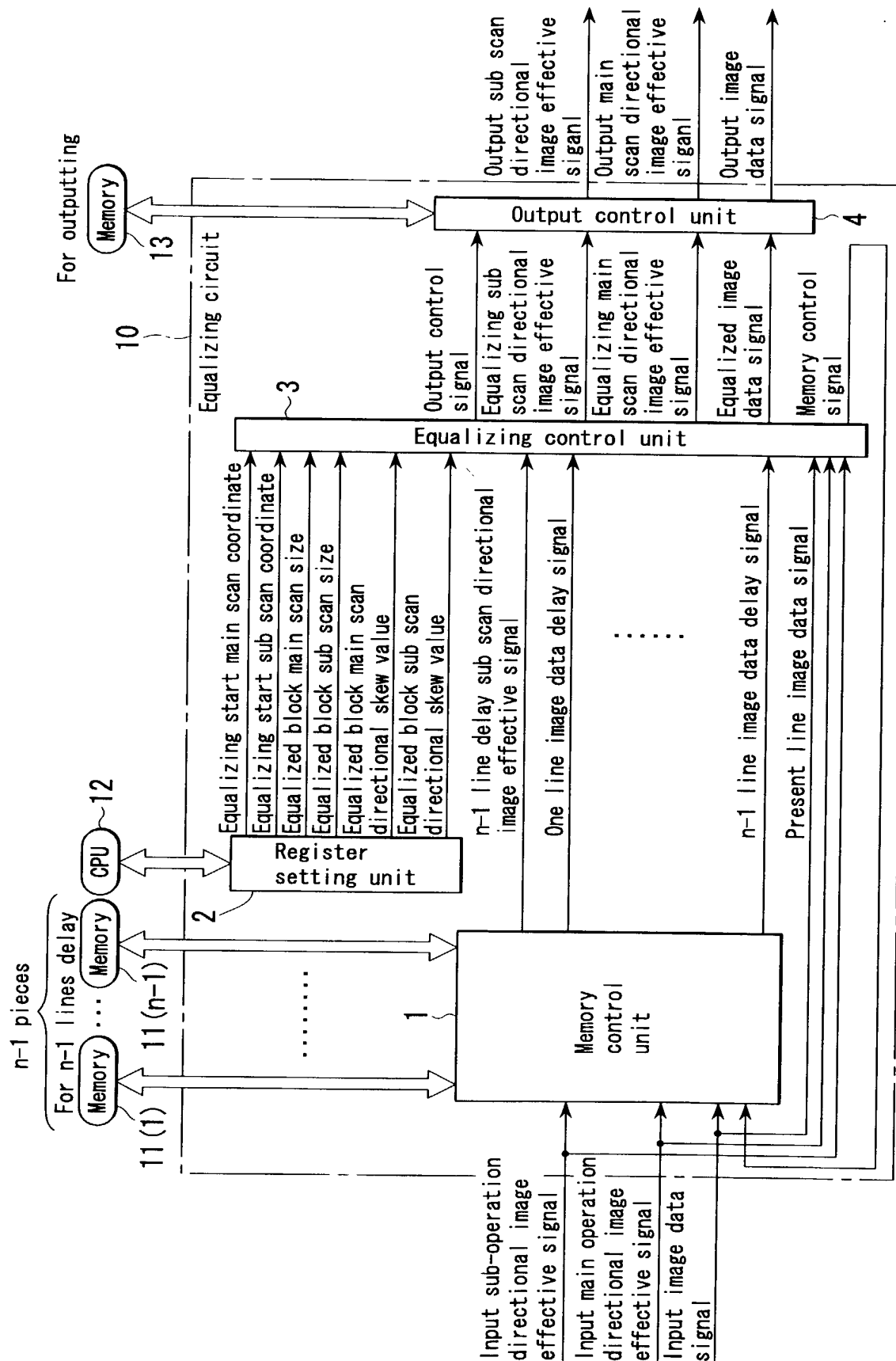


FIG. 5

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Appl. No.: 10/055,402

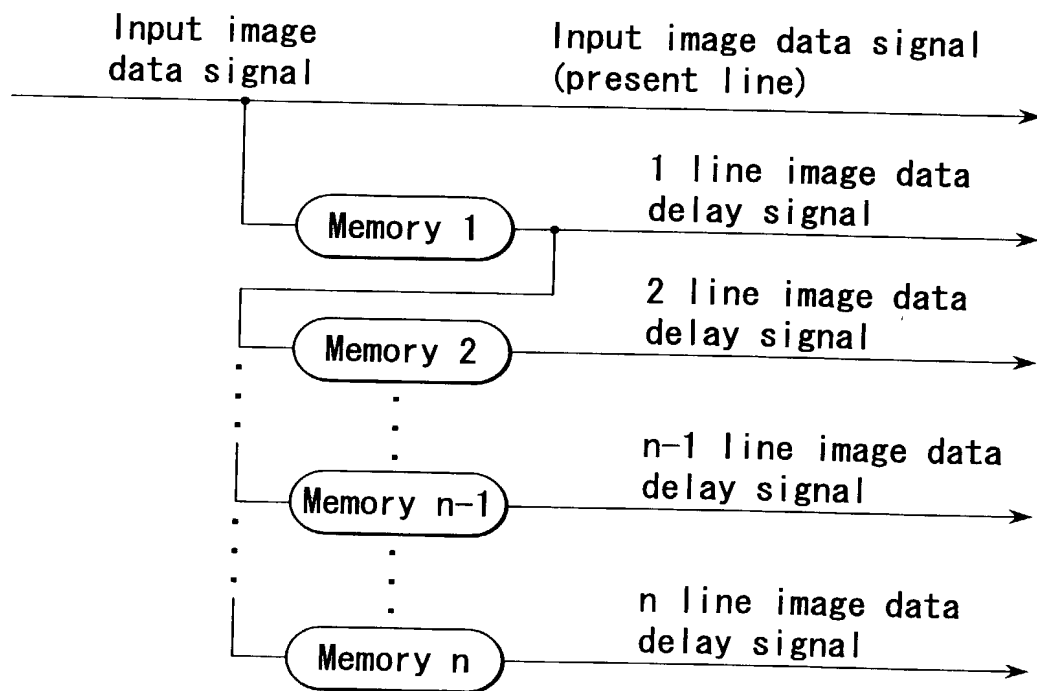


FIG. 6A

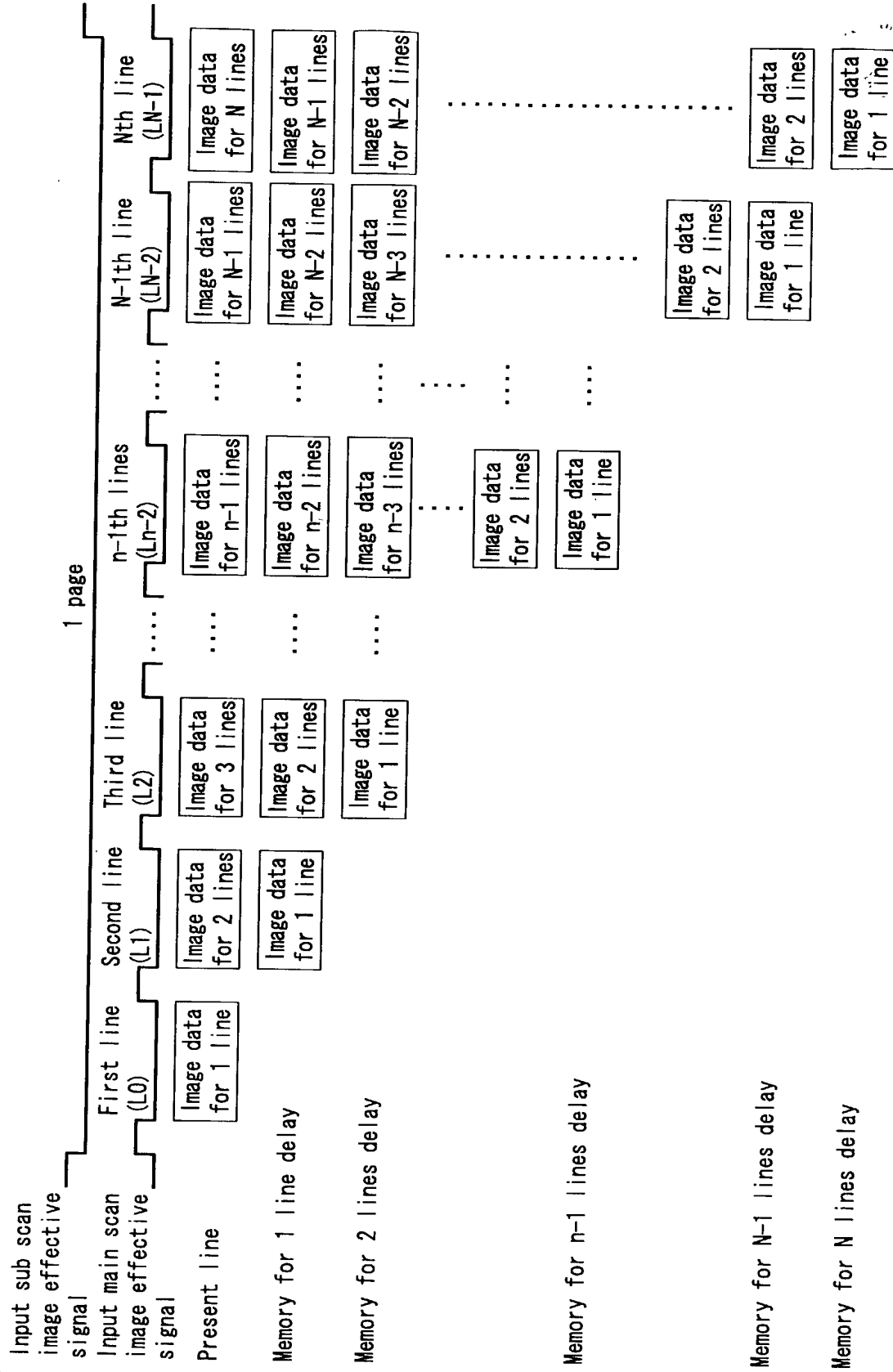


FIG. 6B

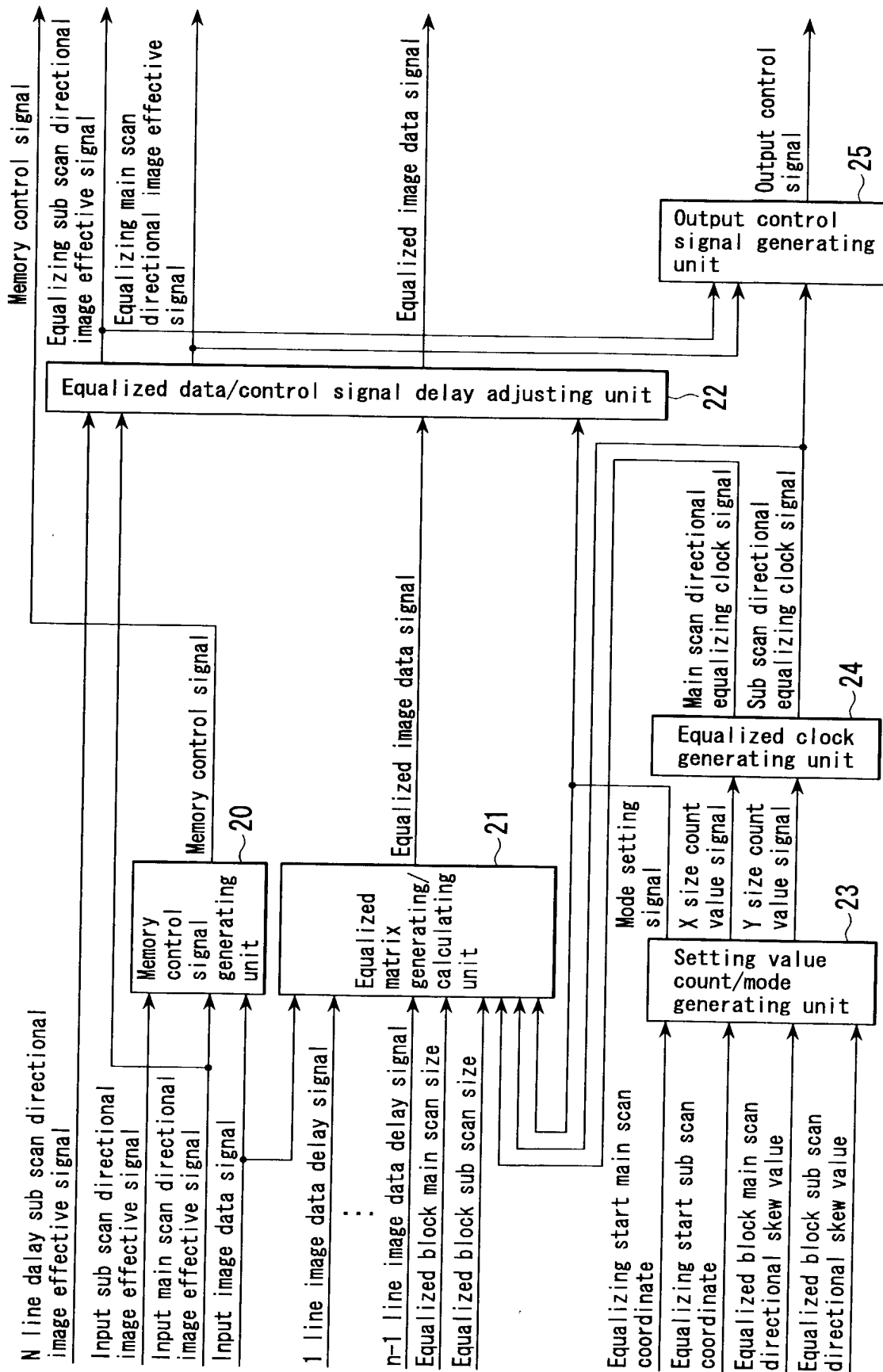


FIG. 7

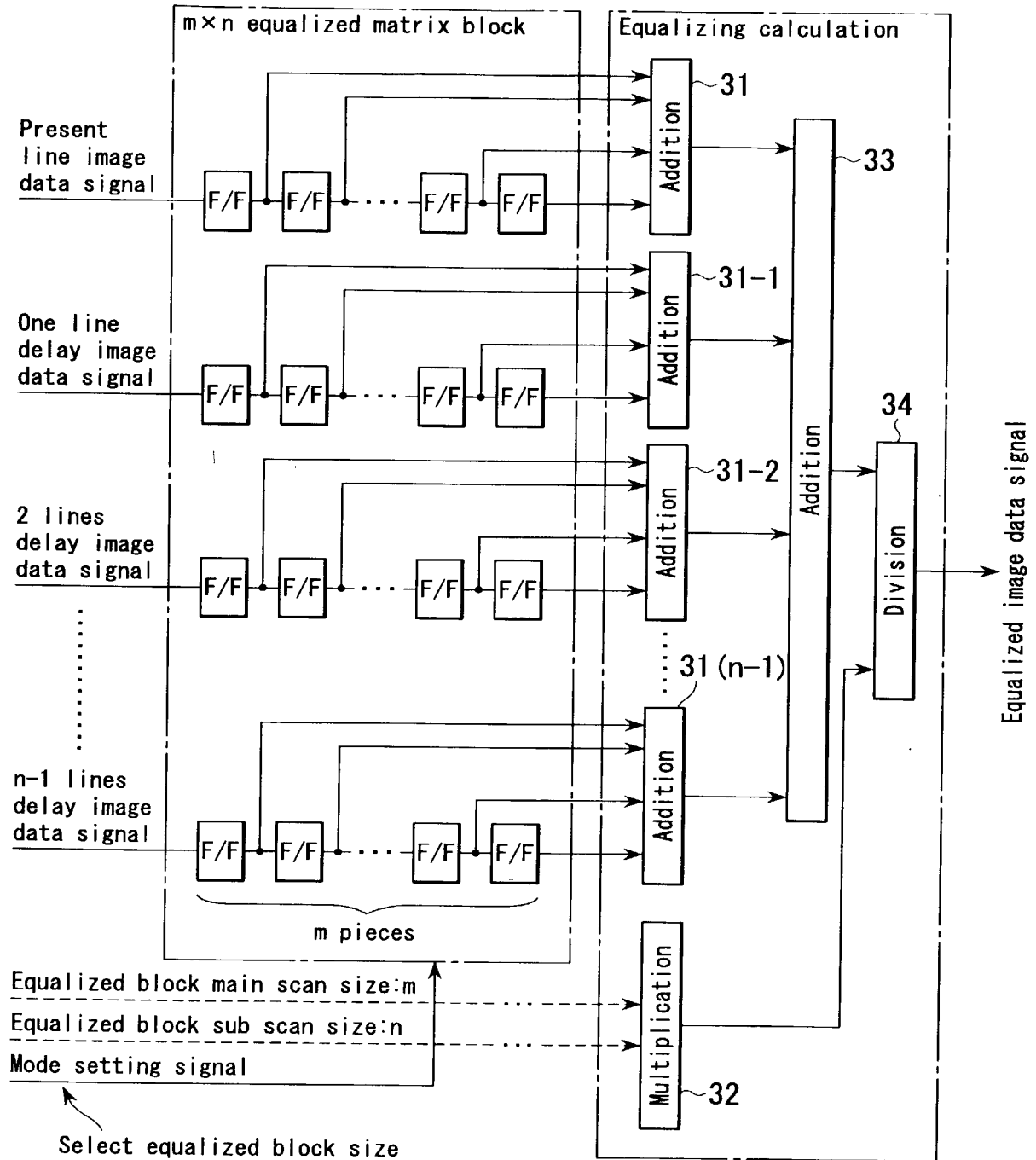


FIG. 8

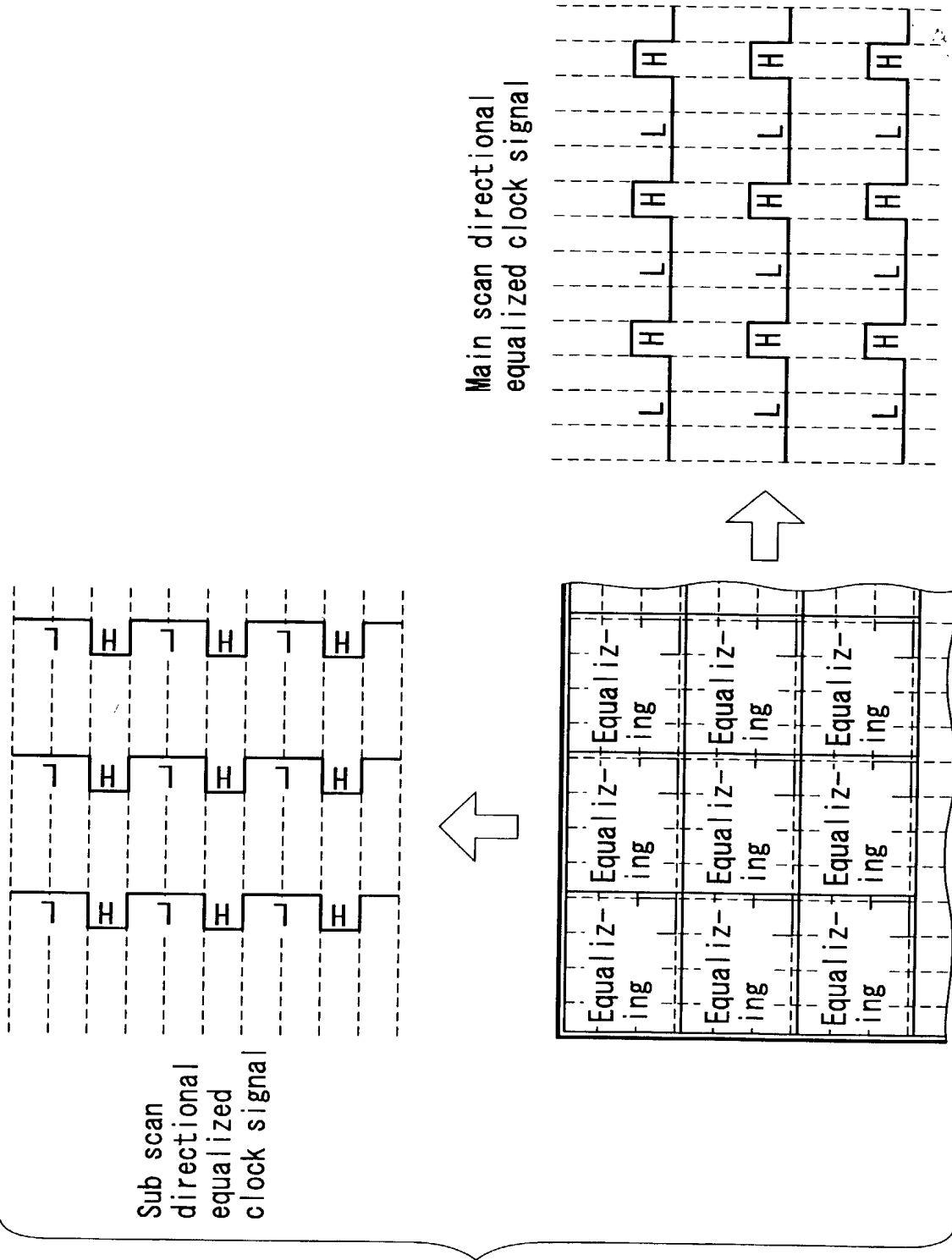


FIG. 9A

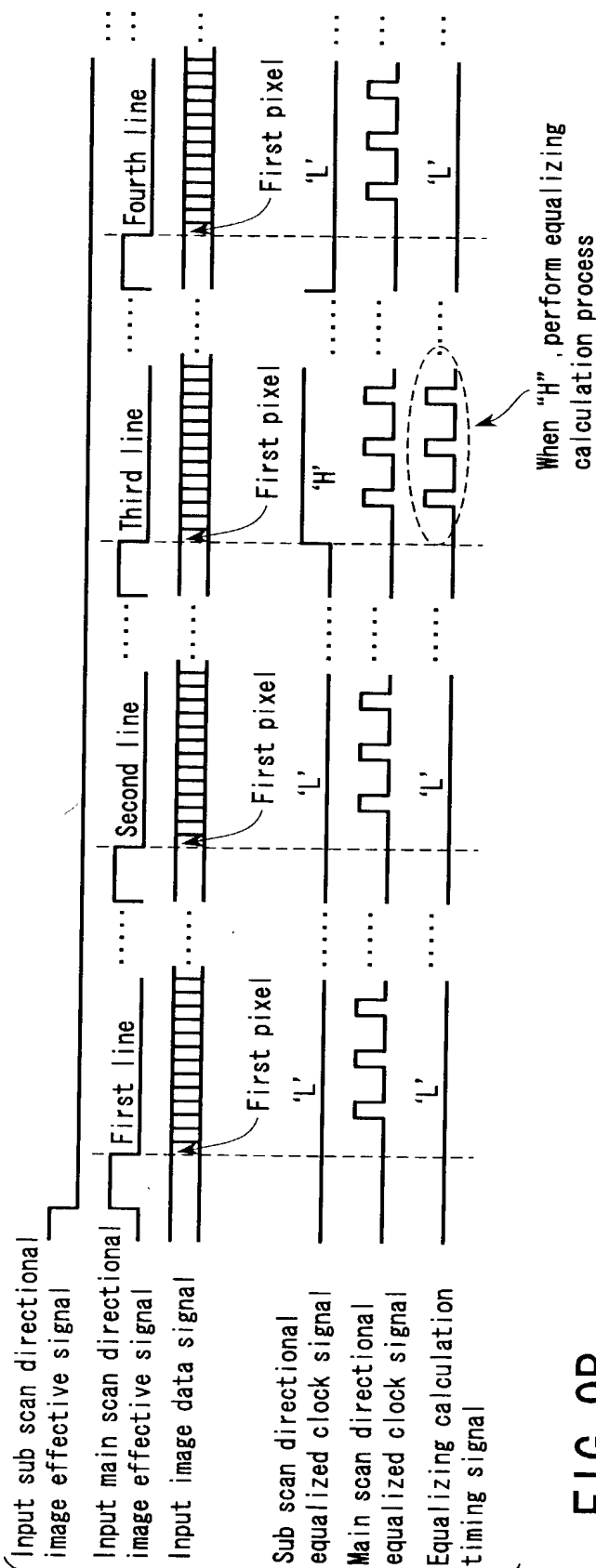


FIG. 9B

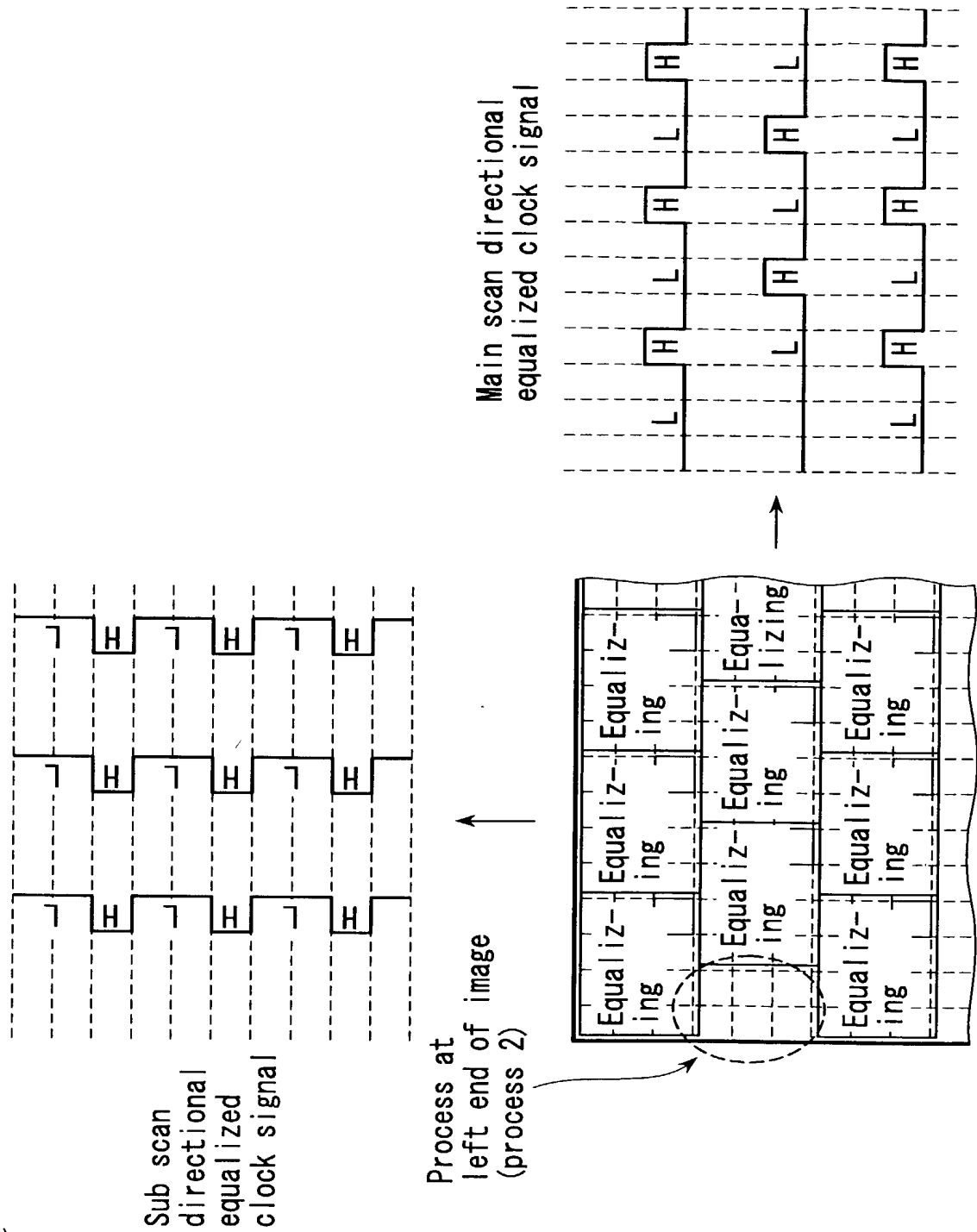


FIG. 10A

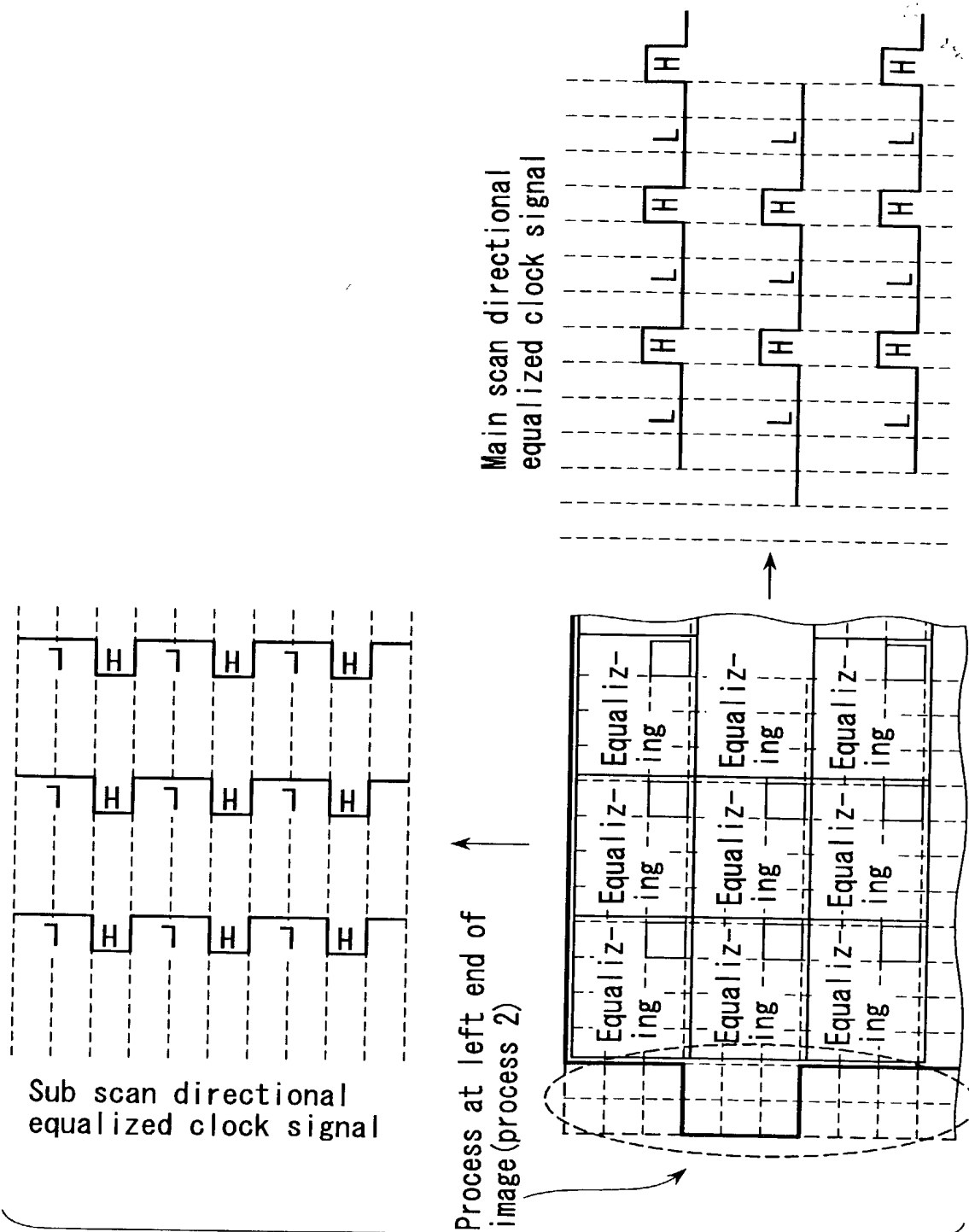


FIG. 10B

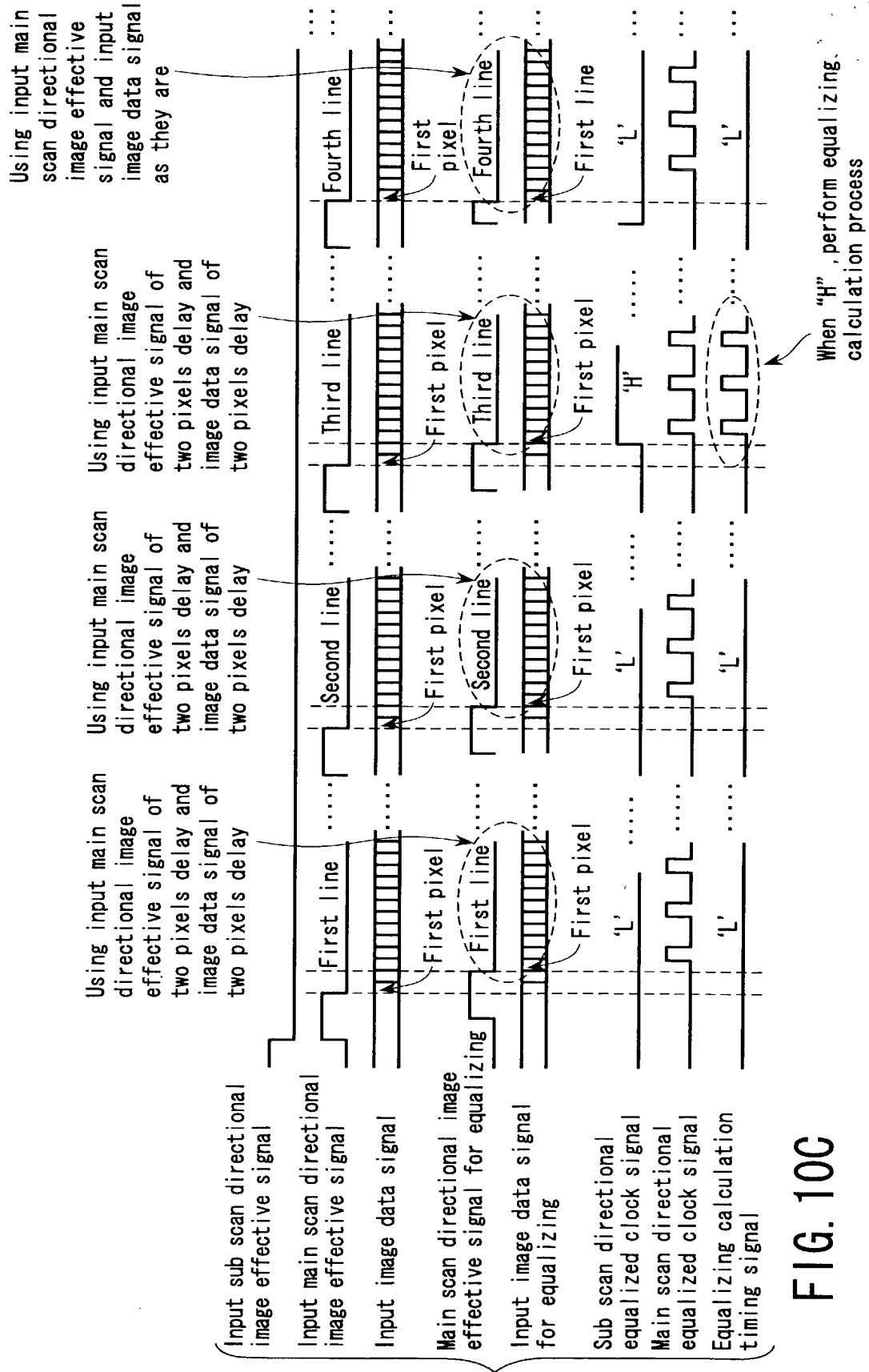


FIG. 10C

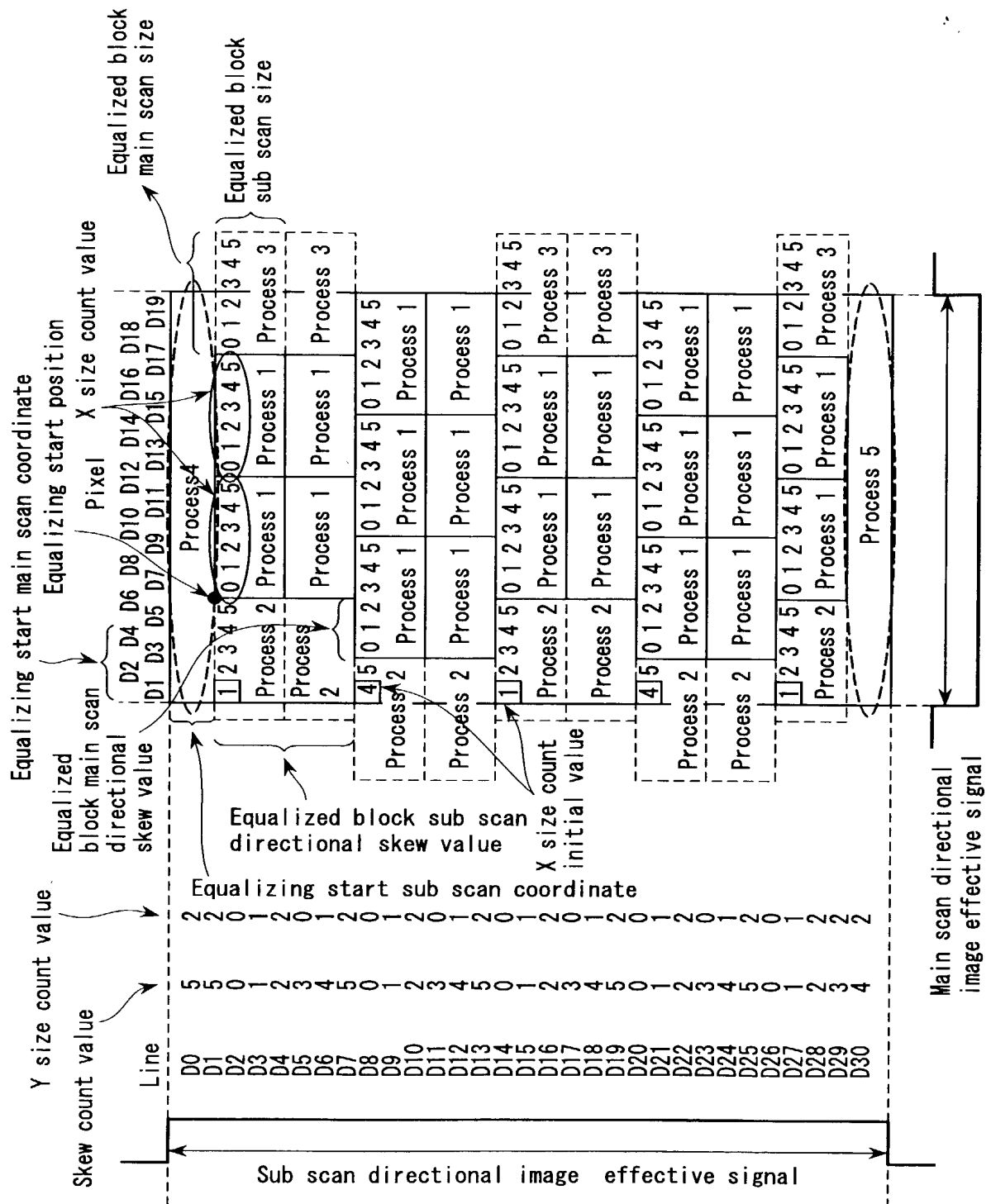


FIG. 11

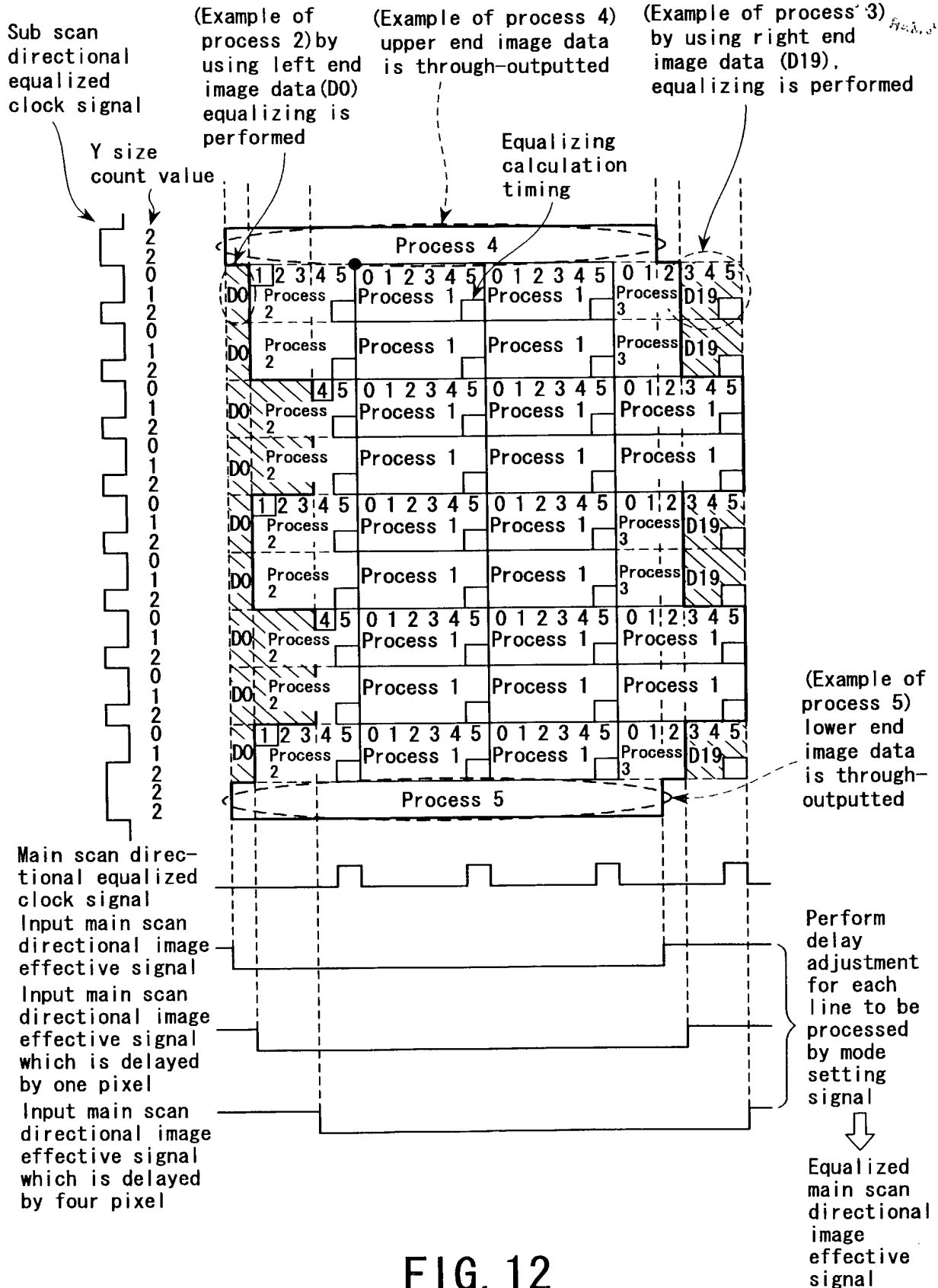


FIG. 12

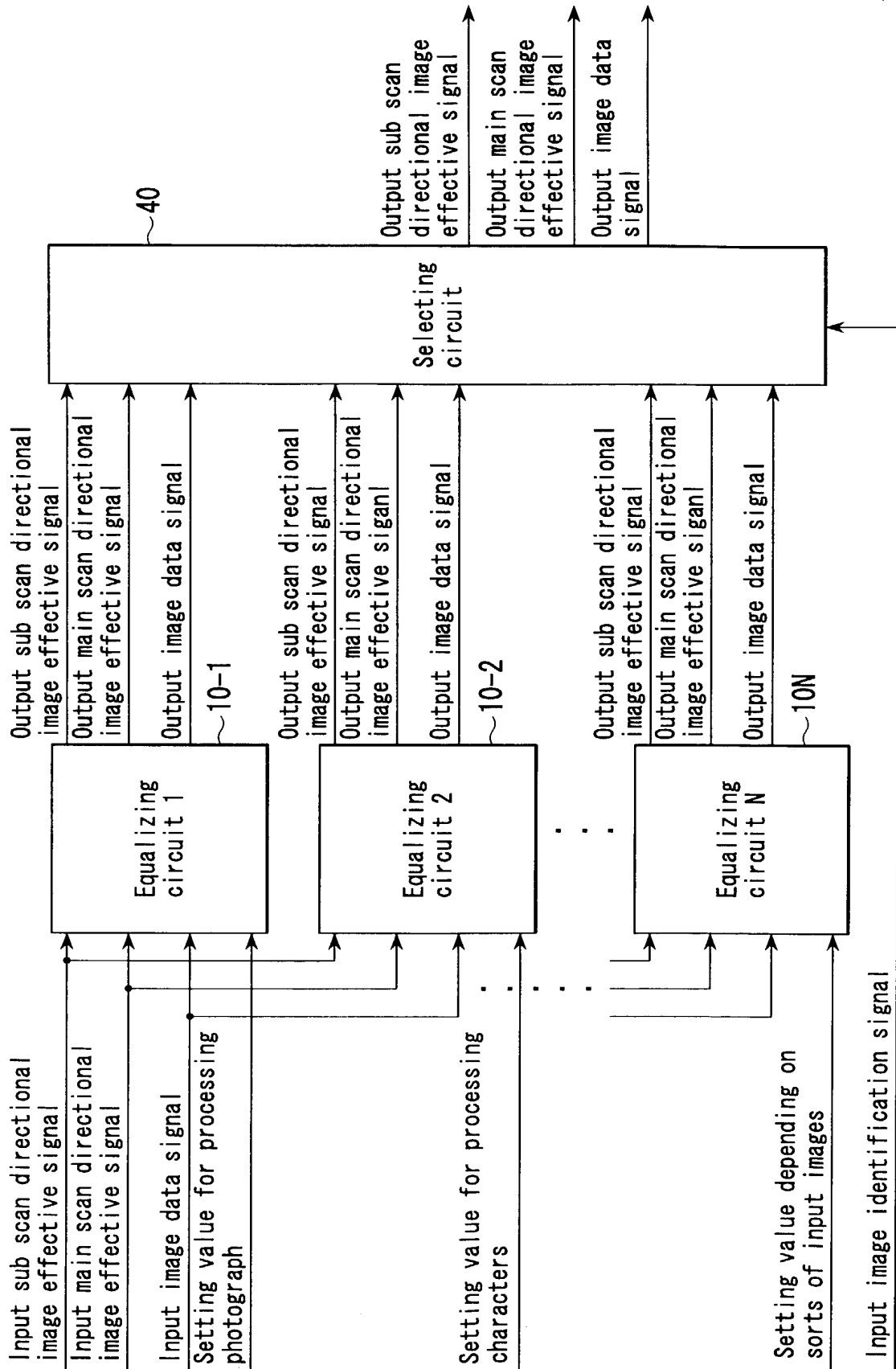


FIG. 13

Image are identified by this signal as photograph and characters

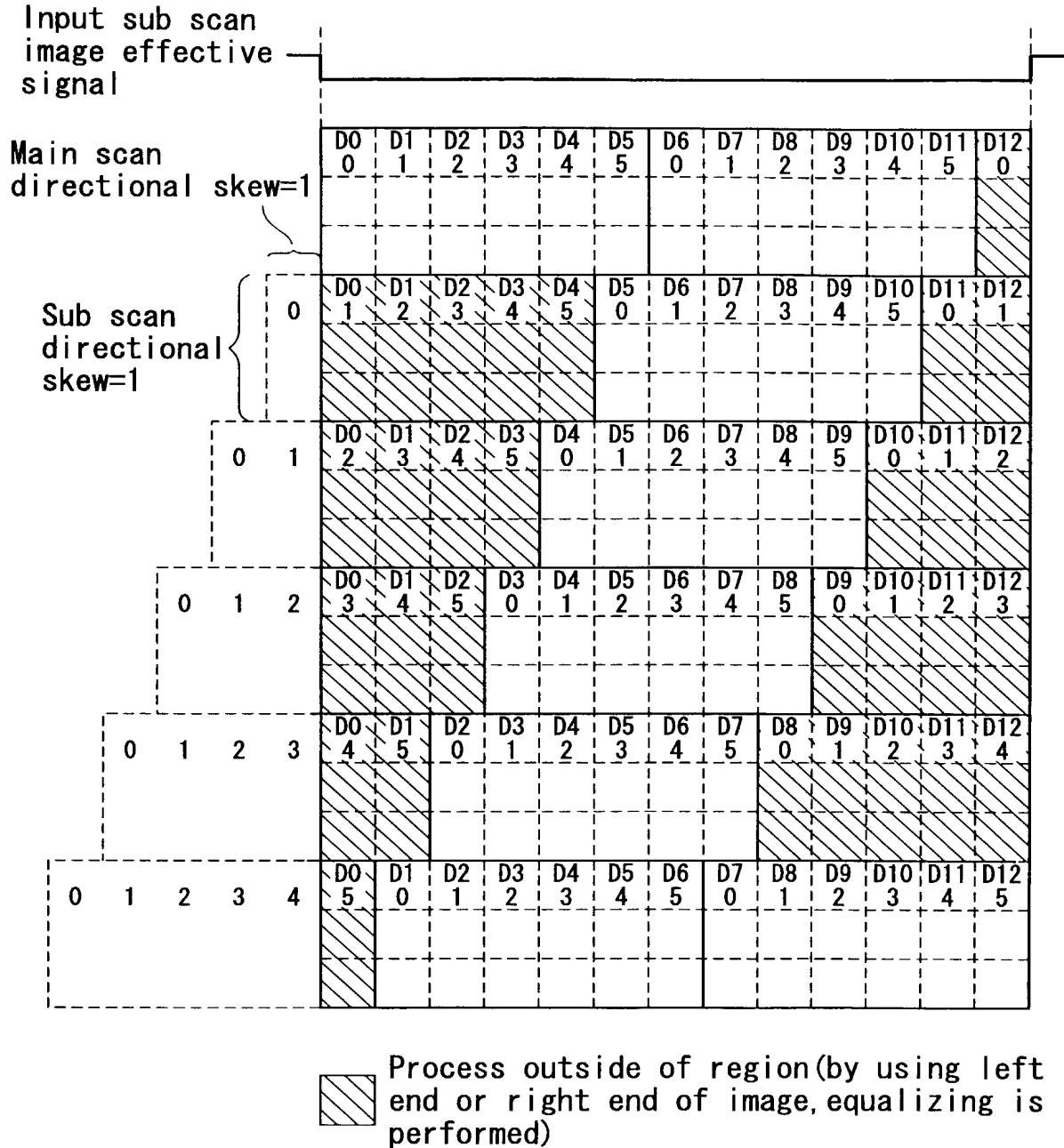


FIG. 14

Input sub scan
image effective
signal

Input image data
signal (1 to 3 lines)

Main scan directional
equalized clock signal

Equalized main scan
directional image
effective signal

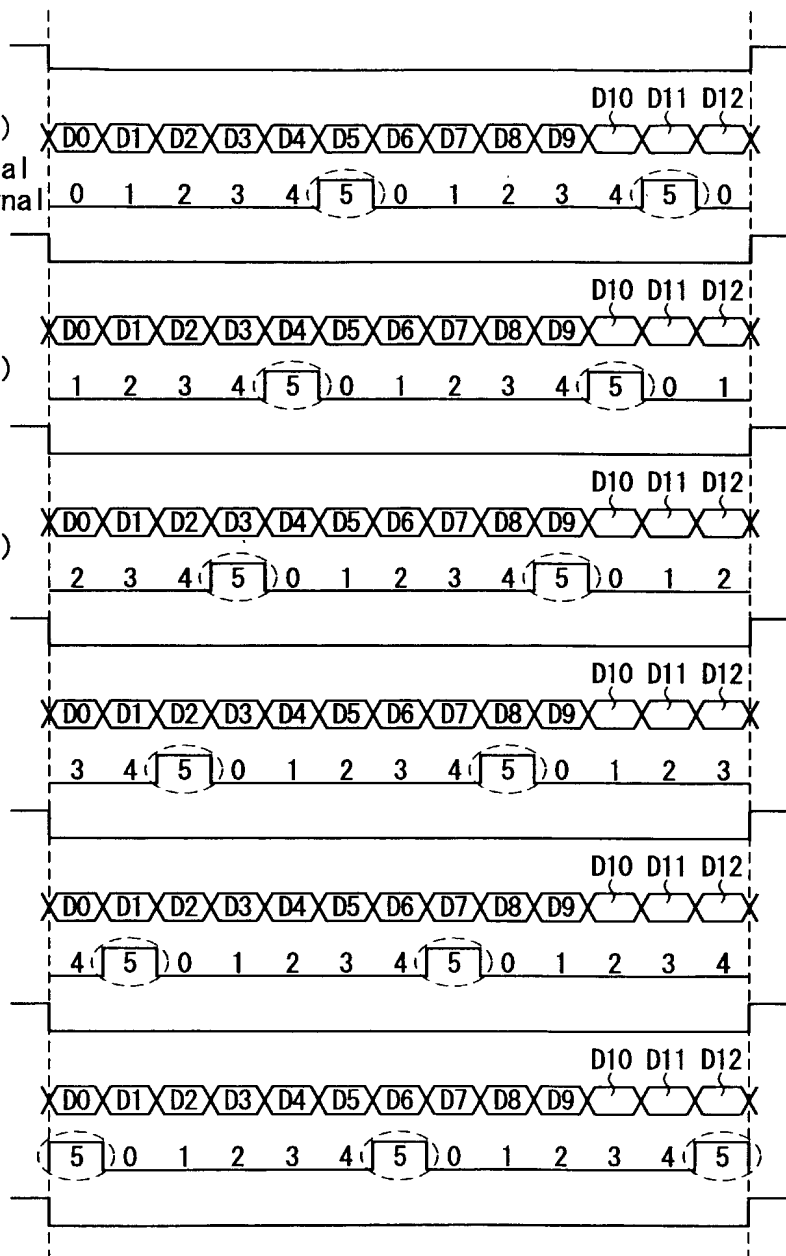
Input image data
signal (4 to 6 lines)

Input image data
signal (7 to 9 lines)

Input image data
signal
(10 to 12 lines)

Input image data
signal
(13 to 15 lines)

Input image data
signal
(16 to 18 lines)



Equalizing calculation timing is different depending on line

FIG. 15

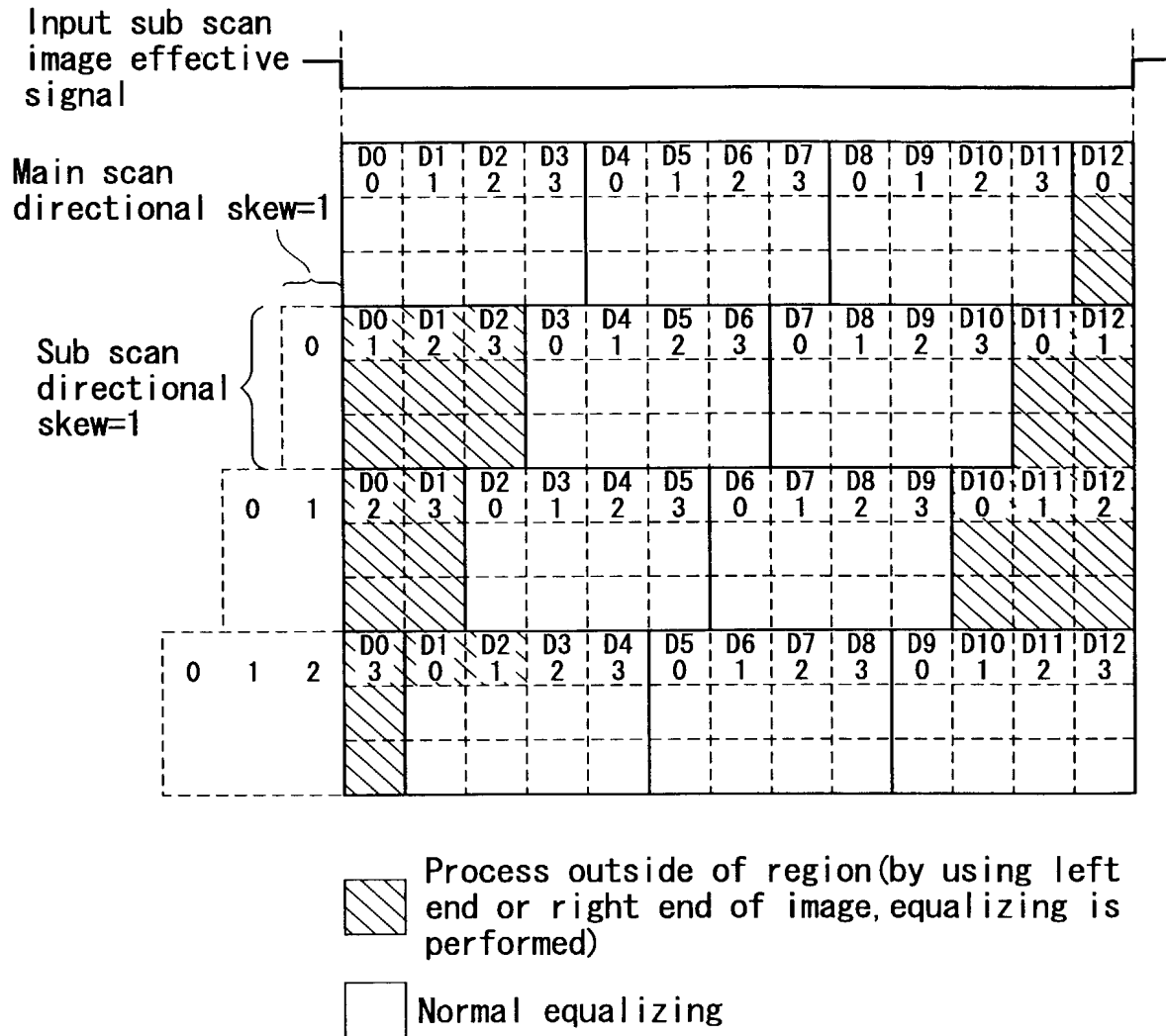
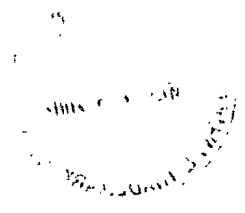


FIG. 16



Equalizing
 calculation
 timing is
 different
 depending
 on line

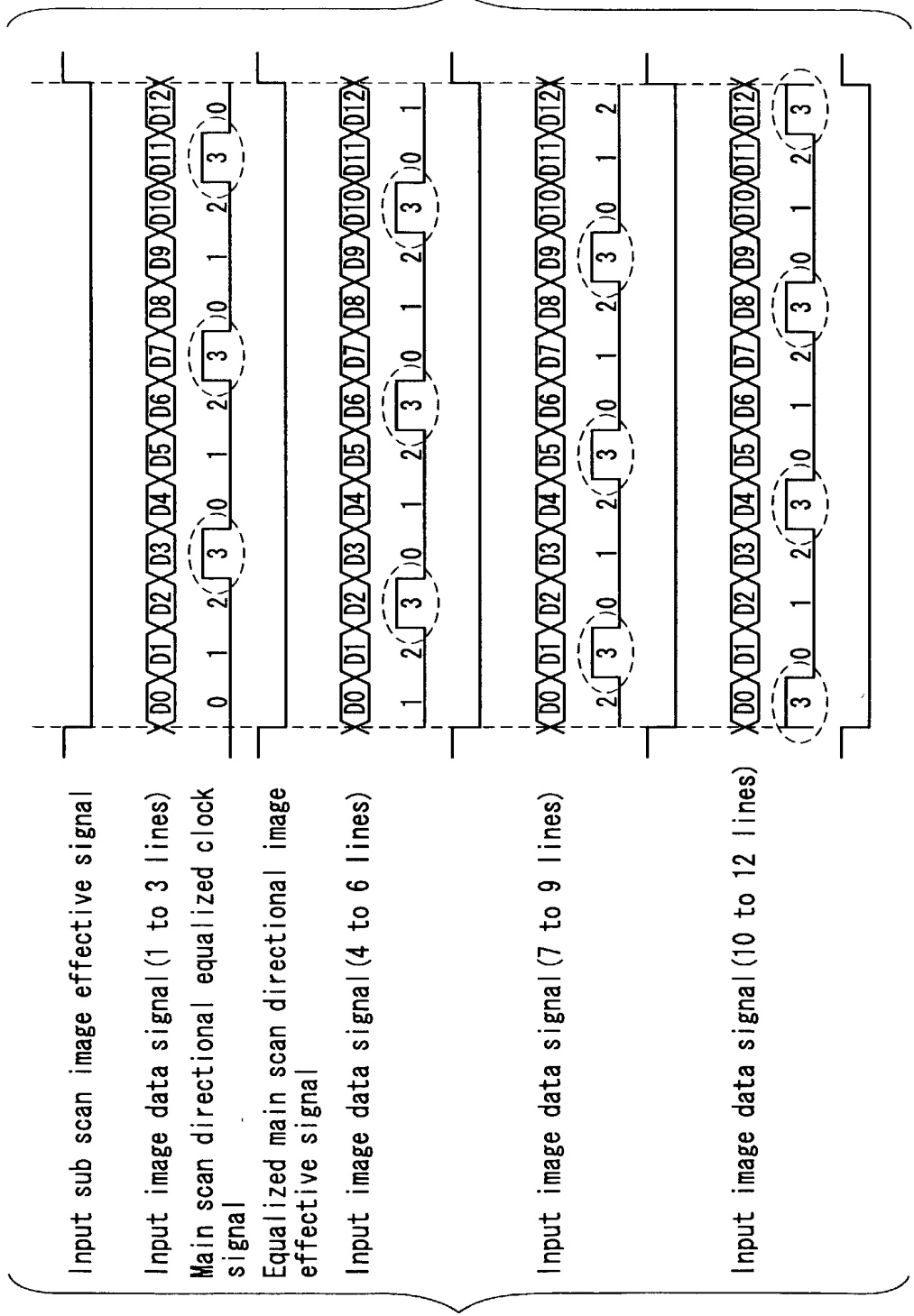


FIG. 17

with a lot of
the same kind of
the same kind of

Input sub scan image effective signal

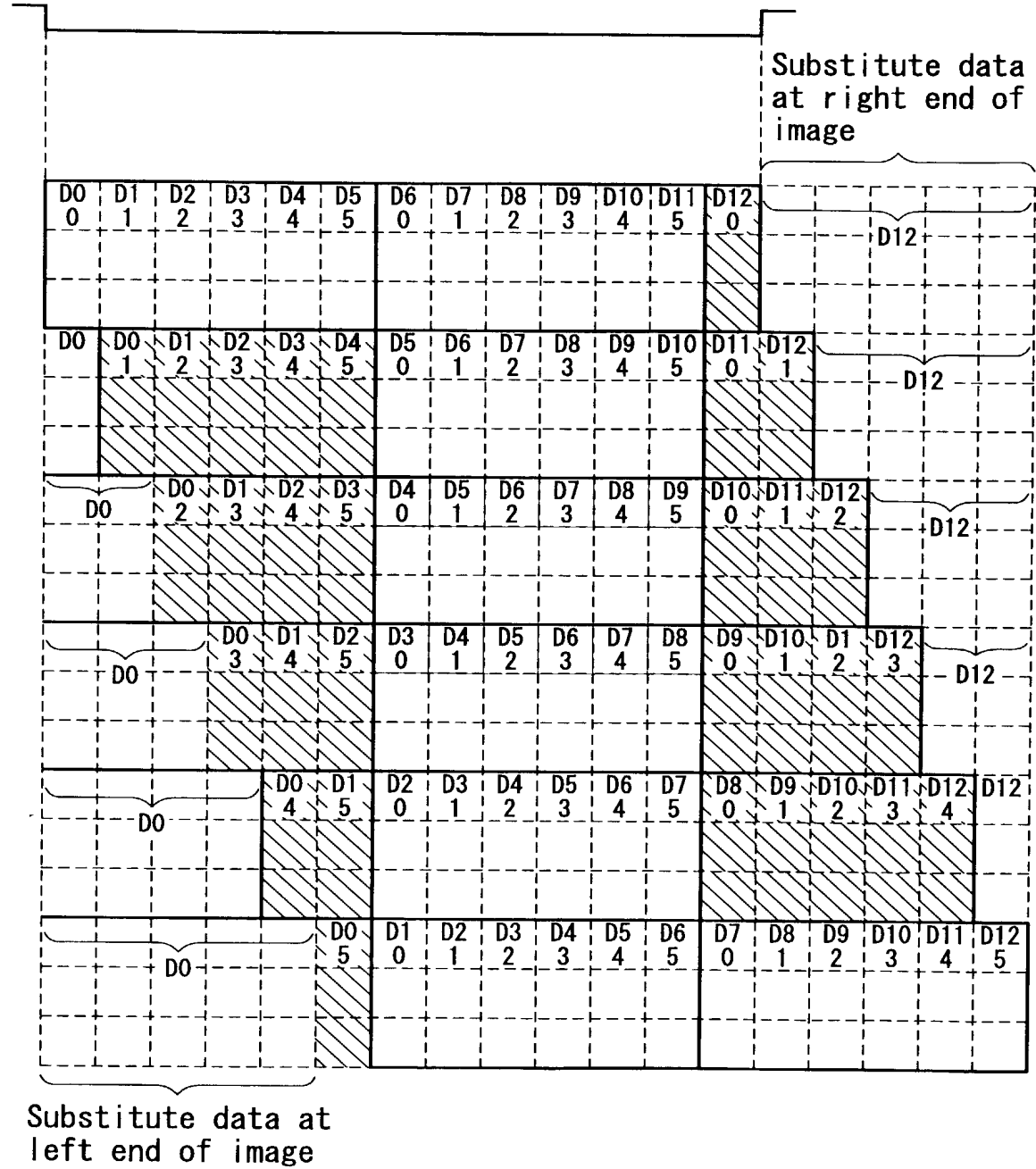


FIG. 18

Delay adjustment is performed for each line to be processed

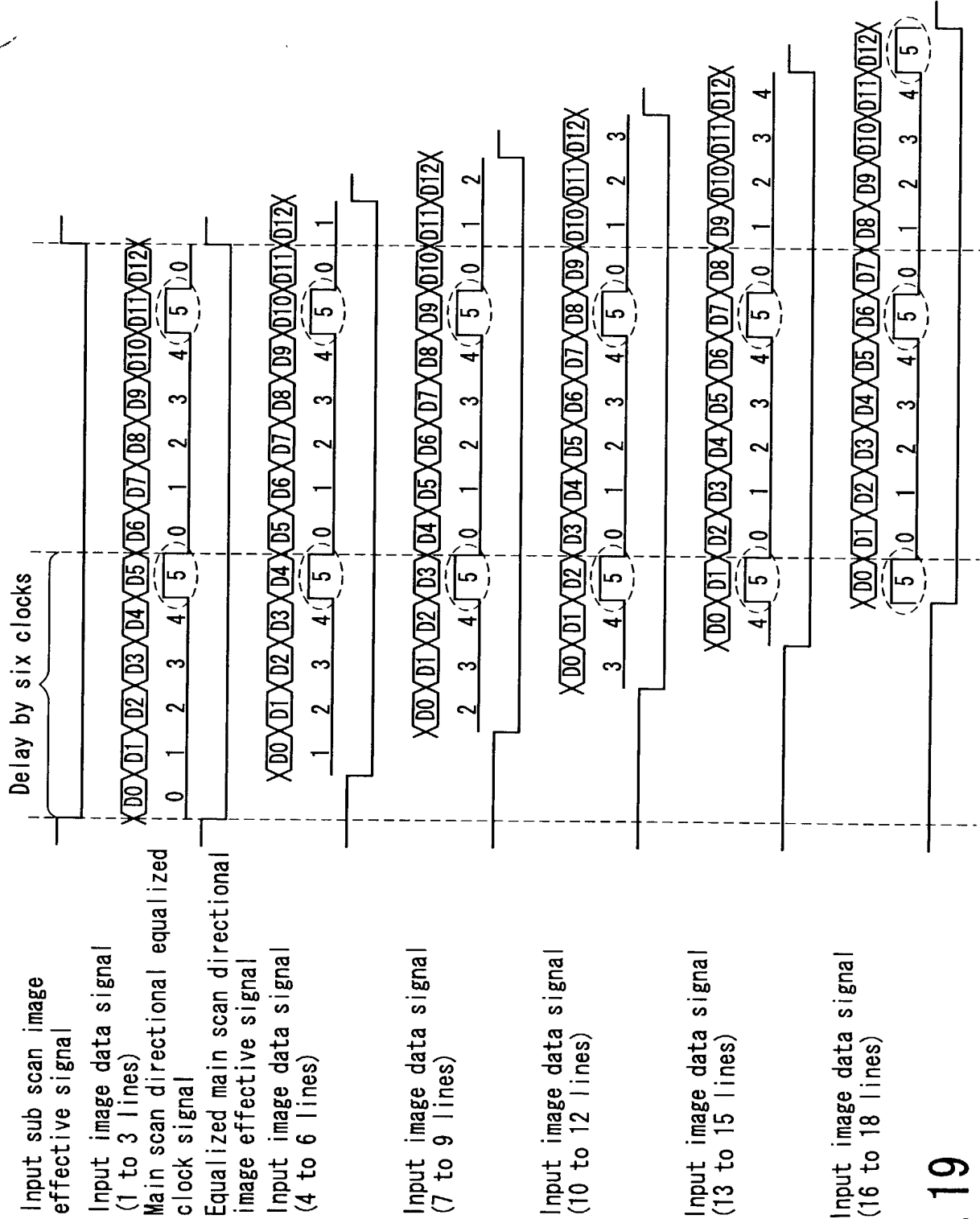


FIG. 19

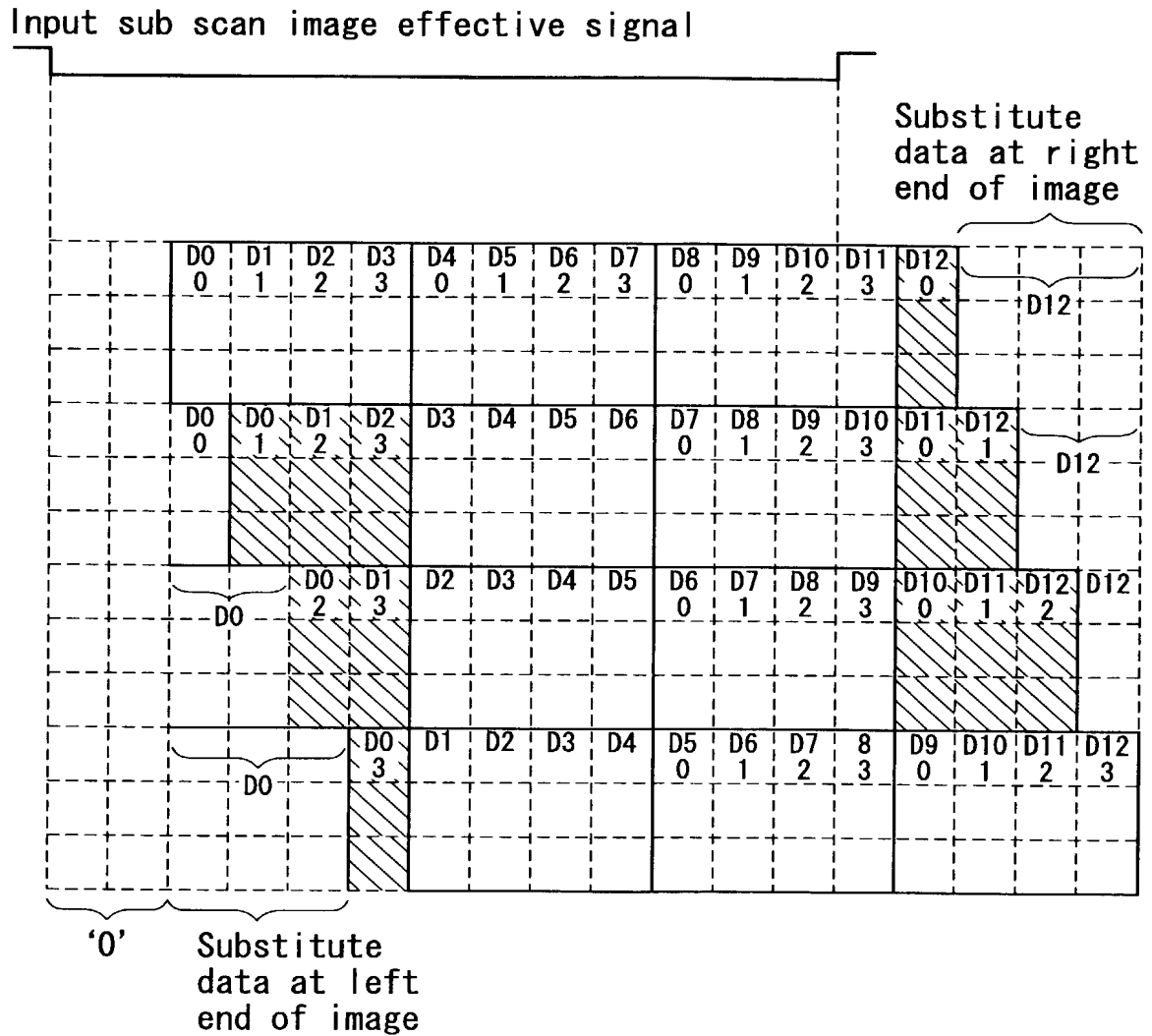


FIG. 20

Delay adjustment is performed
for each line to be processed

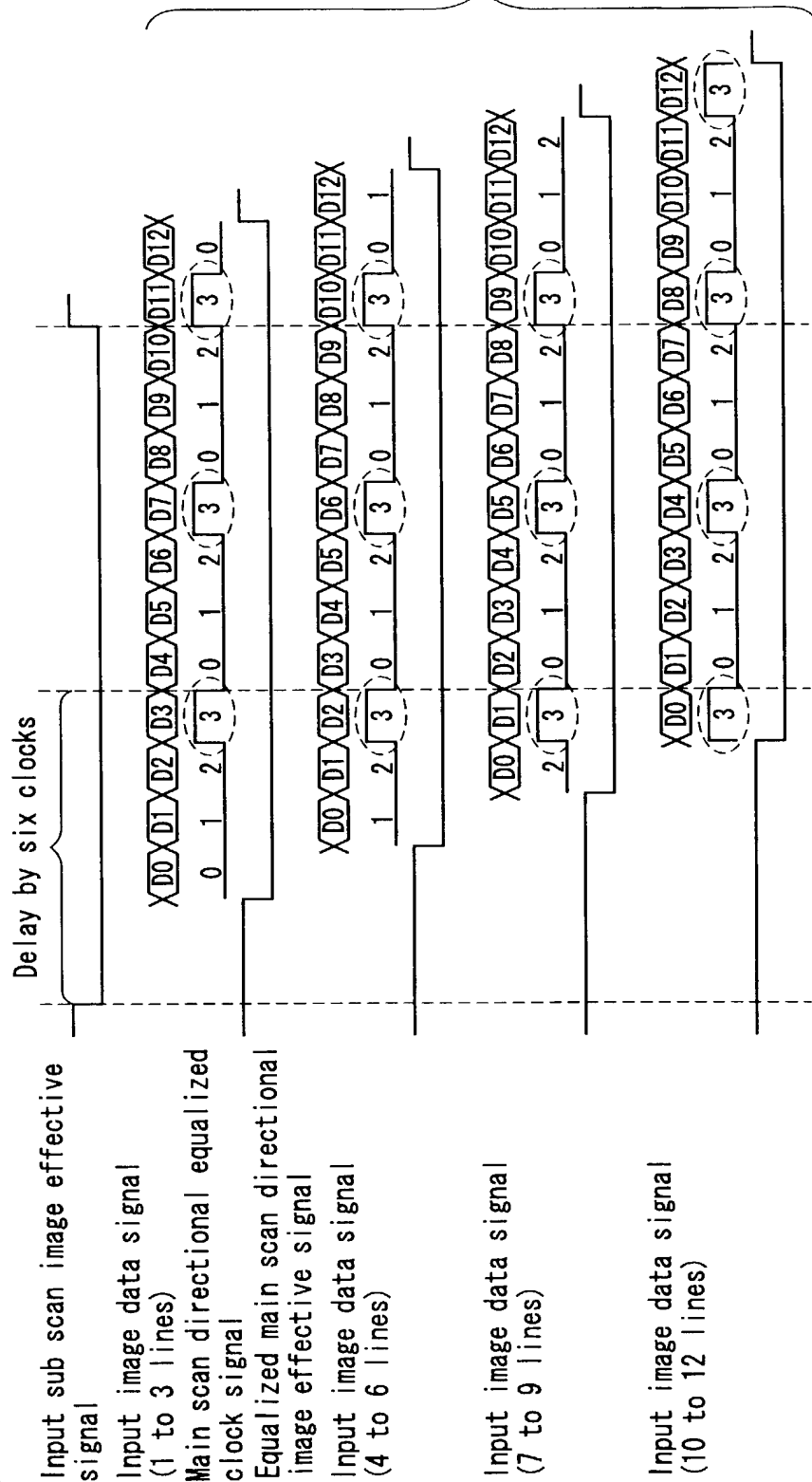


FIG. 21

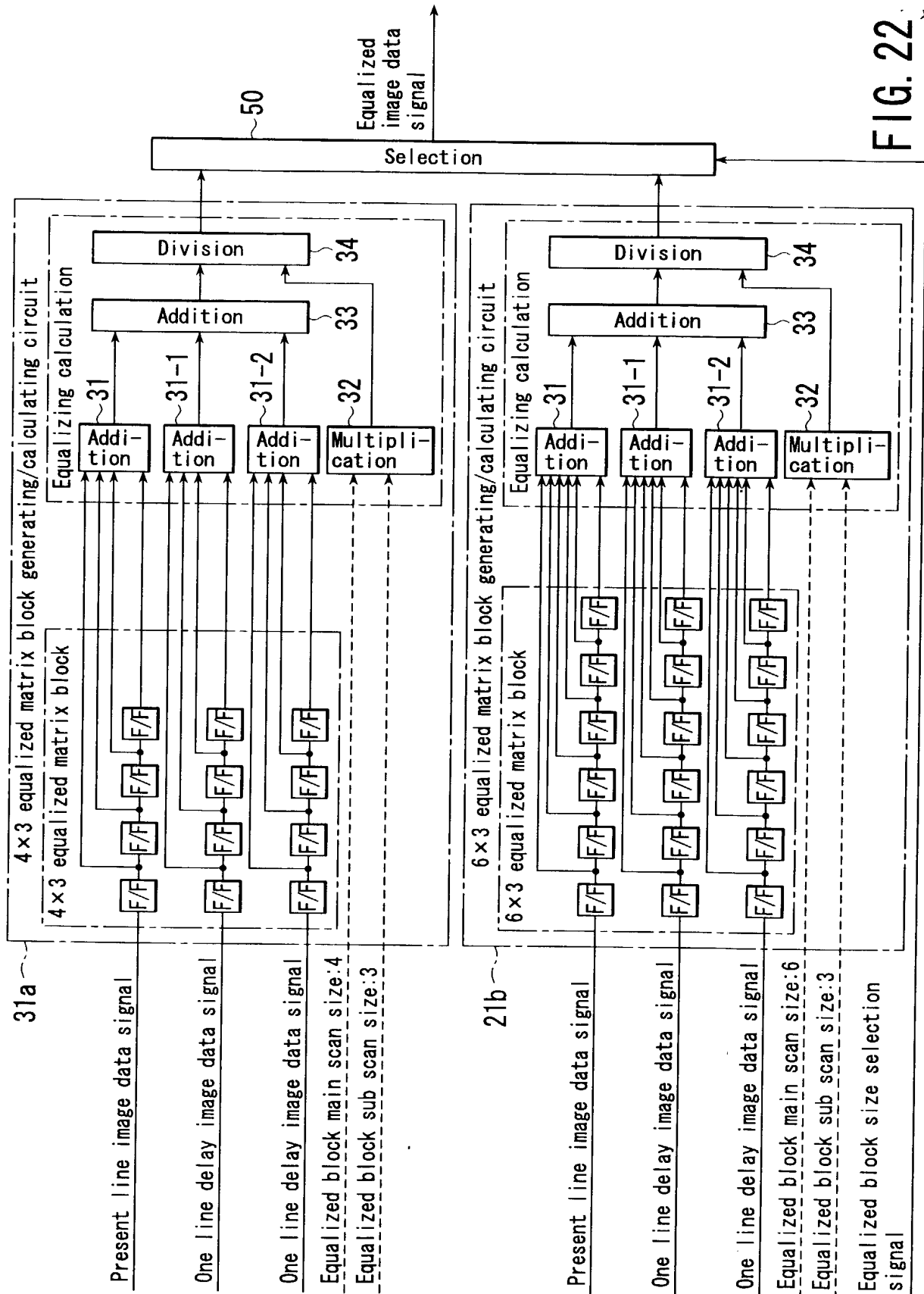


FIG. 22

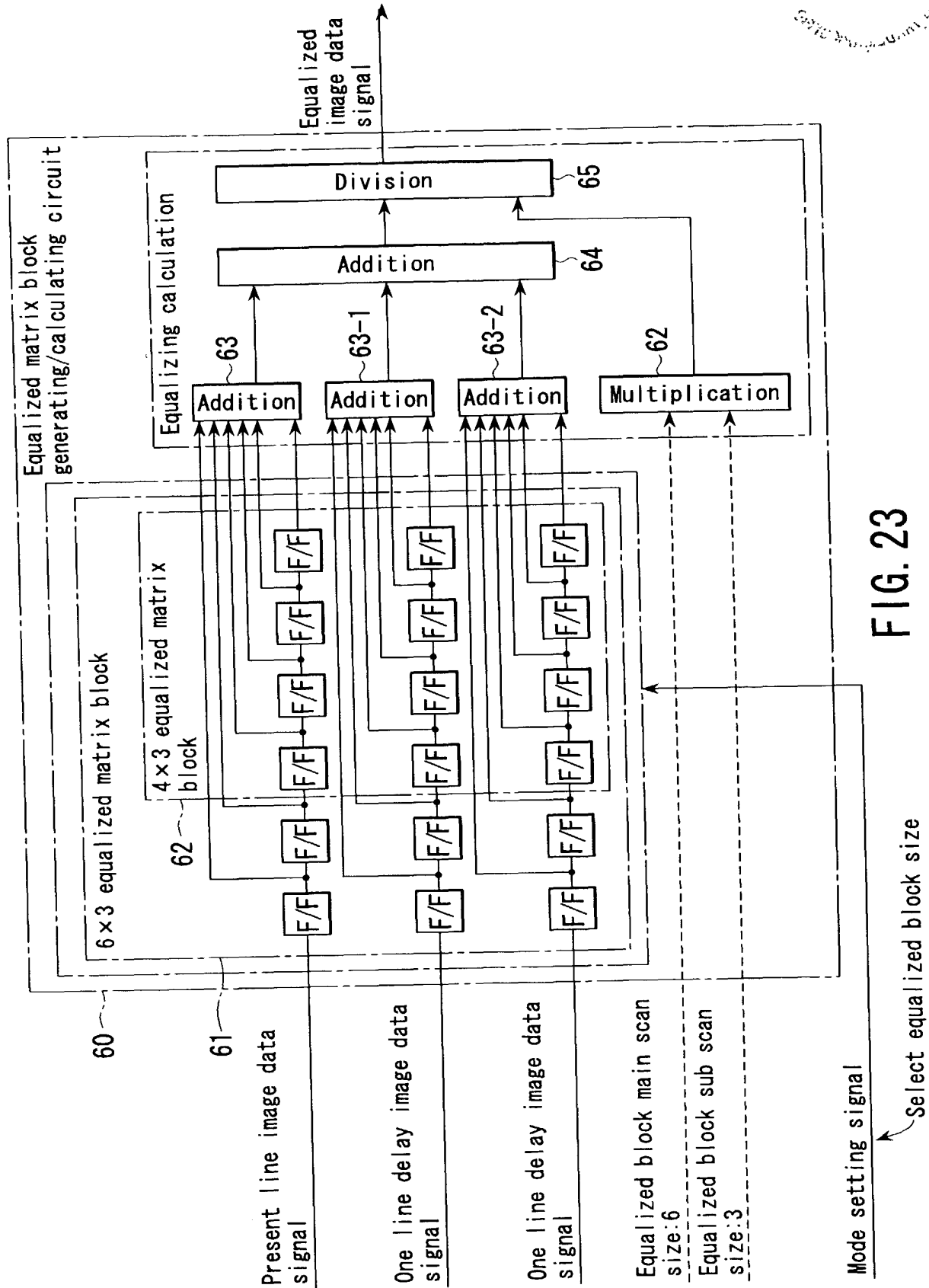


FIG. 23